Latent Damage in CMOS Devices from Single-Event Latchup

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***Abstract*—Evaluation of several types of CMOS devices after non-destructive latchup revealed structural changes in interconnects that appears to be due to localized ejection of part of the metallization due to melting. This is a potential reliability hazard for CMOS devices because it creates localized voids within interconnects that reduce the cross section by one to two orders of magnitude in the damaged region. These effects must be considered when testing devices for damage from latchup, as well as in establishing limits for current detection and shutdown as a means of latchup protection.**

I. Introduction

RADIATION effects on microelectronics are an important reliability issue for many space applications. In particular, single-event latchup (SEL) susceptibility is often considered sufficient reason to not use a device in space. However, because of the recent emphasis on cost reduction, latchup sensitive devices are sometimes flown in conjunction with mitigation hardware or software [1-5]. As noted in [4], a recent series of low-cost satellites has allowed the use of latchup-sensitive parts provided a suitable latchup protection circuit is used.

It is important to know the behavior of such devices during latchup in order to effectively circumvent failure when mitigation circuits are used that detect latchup, and then shut down power to the device. The current detection level and the time that the latchup persists before shutdown are both important, and must be capable of mitigating latchup damage in devices that may have large numbers of internal locations that are sensitive to latchup. This study discusses recent observations of changes in metallization from SEL that affect the integrity of interconnects and can potentially cause damage at a later time from normal current flow, even though the circuit continues to operate after power cycling. We define "latent damage" as structural damage which causes no electrically observable parametric or catastrophic device failure, but can be detected by surface analysis using optical or scanning electron microscopy. Latent damage was observed in several CMOS device types and represents a possible reliability hazard that adds an additional layer of complexity to latchup tests of devices for use in space.

A previous study of Analog Device's AD9260 described the initial observation of catastrophic and latent structural damage from SEL during heavy ion and laser testing [6]. The results of that study created an interest in investigating similar behavior in a broad range of CMOS devices, since CMOS technology is susceptible to SEL from the heavy ions in space environments.

This paper emphasizes results for several device types that remained functional despite significant structural damage to their interconnects from SEL. A detailed description of the characteristic physical signatures of latent damage is included, along with key parameters of these types of events. An explanation of why some structurally damaging latchup events are non-catastrophic is presented, along with the threshold current density for damage.

II. Experimental

A. Basic Test Methods

Six types of CMOS devices were studied for SEL-induced structural damage. All six device types experienced catastrophic structural damage and device failure when they were thoroughly evaluated, subjecting them to at least 20 latchups (with a current limited power supply). However, three types also exhibited "latent damage"- structural damage that did not cause device failure or malfunction - after some latchup events, giving the false impression that no damage had occurred. Table 1 lists the studied devices and their susceptibility to latent damage determined to date.

Californium-252 fission fragments were used to induce latchup on delidded devices in vacuum. All supply voltages were within normal operating ranges, and normal operating currents of all of the devices were low enough so that additional heating of the device within the vacuum system was unimportant. The mean time between latchup events was five minutes to several hours, depending on the device type.

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The low latchup rate and rapid current shutdown eliminated concerns about excess heating during the tests.

A Hewlett-Packard 6629 power supply was used to supply power, with separate force and sense lines. This power supply can measure currents as low as 100 µA. Current limiting can be set over a wide range, with a maximum current of 2 A. The power supply will shut down in < 3 ms after the current exceeds the programmed limit. Bypass capacitors on the test fixtures extend the shutdown time; this depends on the capacitance as well as the magnitude of the current during latchup. It was about 5 ms for devices with on-board capacitors of 10 µF (assuming a nominal latchup current of 100 mA), but could be reduced to 0.1 ms or less for test fixtures with small bypass capacitors. Several of the test fixtures required high values of capacitance in order to maintain stable electrical operation, restricting the time interval for power shutdown. More specific details of the test approach for each type of device are given below.

TABLE I
CMOS DEVICES STUDIED FOR SEL-INDUCED DAMAGE

Device	Device Type	Manufacturer	Latent Damage	Catastrophic Damage
AD9260	ADC	Analog Devices	Yes	Yes
AD9240	ADC	Analog Devices	No	Yes
ADC10321	ADC	NSC	Yes	Yes
CAR/CPPX1T-A7BR	Oscillator	Cardinal/Cypress Hybrid	Yes	Yes
LTC1799	Oscillator	Linear Technology	No	Yes
ADSP2100	DSP	Analog Devices	No	Yes

Analog-to-Digital Converters

Analog-to-digital converter tests were done on special evaluation boards, obtained from the manufacturer. These boards all required large capacitor values. A sinusoidal input signal was applied during the tests, comparing it with a reconstructed analog output signal (from the digital outputs, through an external digital-to-analog converter) to monitor device functionality. The reconstructed sinusoidal output fell to zero whenever latchup occurred. If the latchup was not destructive, the waveform was normal after power cycling.

The current was continually monitored, and recorded on a computer. In some of the tests detailed waveforms of current pulses were measured with an oscilloscope through a series resistor. The current waveforms showed that a steady state current value was reached in < 100 µs, and that it remained nearly constant until the power supply was shut down.

Oscillators

Functional testing of the programmable oscillators was straightforward. The output of the oscillators was continually monitored with an oscilloscope, measuring oscillator frequency continually with the internal analysis provided on the oscilloscope. For non-destructive latchup events, the device continued to operate with no change in frequency, although there was a large increase in power supply current (up to 1 A), compared to normal operating currents of about 15 mA.

For destructive latchup events, the oscillators often continued to operate, but there was a large change in frequency. This change in frequency remained after power was removed and reapplied. In other cases, a complete loss of output signal was observed following destructive latchup events.

Digital Signal Processor

During latchup testing the digital signal processor was in a primitive operating mode, using a clock input, but without a specific series of operations. Although this approach would not work for conventional SEU testing, it appeared to be adequate for latchup testing (system tests done at a later date with a fully operating DSP yielded similar results for latchup cross sections). After a series of latchup tests, or after a high-current latchup event occurred, the DSP was taken to another laboratory for evaluation in a system application.

Current waveforms were measured for each latchup event using a digital oscilloscope, and stored on a computer for later analysis. Latchup currents ranged from approximately 30 mA to more than 2 A (the maximum current available from the power supply). There were many different latchup paths, making this device particularly difficult to evaluate. These currents are consistent with the conventional view of four-layer latchup, and are clearly not "microlatchup" events, which are more likely due to snapback than latchup [7].

B. Test Approach for Laser Testing

In addition to tests with heavy ions, the AD9260 was used for a special series of tests at The Aerospace Corporation's laser facility that provided more detailed information about latchup sites as well as the time delay between the onset of latchup and the time at which the circuit ceased to operate if the latchup was destructive. None of the other devices were tested with a laser. A different test method was used for the laser tests in order to allow a large number of latchup events to be observed, paying particular attention to restricting the time period over which latchup occurred. Supply currents were measured for each latchup event through a 1-ohm sampling resistor and a differential pre-amplifier made by Tektronix. SEL events were recorded as waveforms in a digital oscilloscope and analyzed via computer software. The devices were irradiated with single 815nm, 1-nJ laser pulses with a 3-4 μm spot size and a 10 ps pulse width. Pulses could be initiated by external control, allowing synchronization of the laser pulse and the device power supply.

The power supply to the DUT was turned on 10 ms before each laser pulse and remained on for 1 ms after the pulse. The power was shut down 1 ms after each laser pulse, regardless of whether latchup occurred. This was done to provide a consistent power time profile when a succession of laser pulses was used in combination with an X-Y stage to "scan" the device and determine which regions were sensitive to latchup. The position of the laser spot was monitored with a viewing screen linked to a CCD camera focused on the devices.

Device functionality was monitored with an oscilloscope. This monitoring system was also used after every laser pulse to determine if catastrophic damage had occurred. The CCD camera allowed latent damage to be detected because the ejected metal spheres could clearly be seen in the metallization regions near the latchup-sensitive region.

C. Diagnostic Approach

Because of the random location of the fission fragments, latchup testing at JPL's Californium-252 facility did not allow direct observation of the region on the device where we were causing latchup-induced damage. This necessitated simultaneous monitoring of the SEL equilibrium current and device functionality one event at a time. After a latchup event, the DUT was removed from the vacuum chamber, and the die was scanned with an optical microscope for potential damage sites. This process was often challenging due to the intricacy of many of the studied circuits and the relatively small sizes of the damage sites. These sites usually appeared as round, shiny regions relative to surrounding material and ranged from approximately 0.5 to 4 micrometers in diameter.

If damage was suspected, the device was evaluated using scanning electron microscopy (SEM). SEM allowed us better resolution and the ability to perform energy dispersive spectroscopy (EDS) where the x-ray spectra of the damage site was matched against the characteristic spectra of various elements.

In order to determine the feature sizes of the interconnects that had been damaged and more clearly observe the structural damage to the metal, plasma etching or acid stripping was used after latchup testing to remove the top layer of insulator material from the die. All of the studied devices were aluminum and Si_3N_4 or aluminum and SiO_2 systems with 2 to 3 levels of metal clad with TiN or TiW refractory metal. Metallization thicknesses prior to damage ranged from 1.0 to 1.2 micrometers, and interconnect widths ranged from 0.9 to 10 micrometers.

As noted above, only catastrophic structural damage was observed for the DSP-2100, AD9240, and LTC1799. However, it is possible that latent damage was present prior to the particular latchup events that caused catastrophic damage in these devices. Optical scanning may have been inadequate for locating latent damage sites in these cases, either because the sites were very small or hidden by slight packaging material remnants that were sometimes not completely removed during the delidding process. Alternatively, latent damage may have occurred in the lower levels of metallization where it would be impossible to observe during optical surface analysis.

III. Results

A. Latent Damage Signatures

Several latent damage signatures emerged that were common to all the device types tested. The round, shiny regions observed optically were found to be spheres of aluminum near significantly voided interconnects. The insulator material surrounding damaged interconnects was often cracked and sometimes fractured and lifted to release metal from underneath. Latent damage most often occurred in the top level of metal, and all tested devices of the same part type were damaged in the same general region of the die. If the region contained replicated structures, then the specific point where latent damage occurred was not necessarily the same for different parts, but could take place in any of the replicated structures. In most cases the ejected material came from extended interconnects (see Fig. 1), with no obvious physical discontinuity (such as corners, vias, or cross overs).

Catastrophic events yielded similar signatures, but interconnect voiding and fracturing was complete in these cases, causing open circuits and device failures.

Fig. 1 shows several latent damage signatures in a still functional AD9260. The three extruded aluminum spheres in the left interconnect created a voided region directly above them. This damage occurred in the top level of metal.

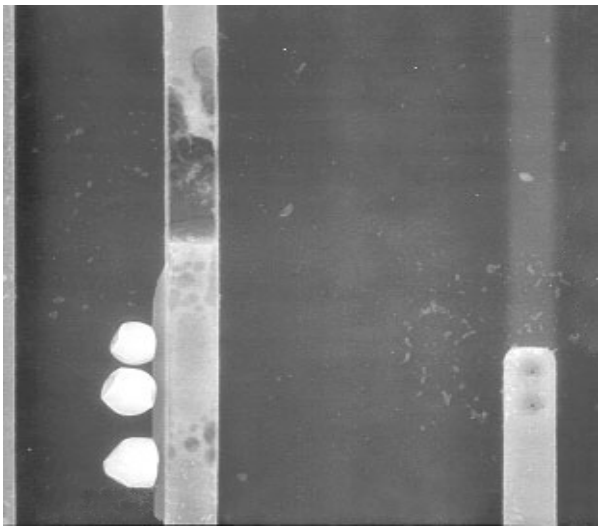

Fig. 1 Scanning electron micrograph of latent damage in an AD9260 with nitride removed.

Fig. 2 shows cracked and lifted insulator material at the site of an erupted metal sphere on a latently damaged National ADC10321.

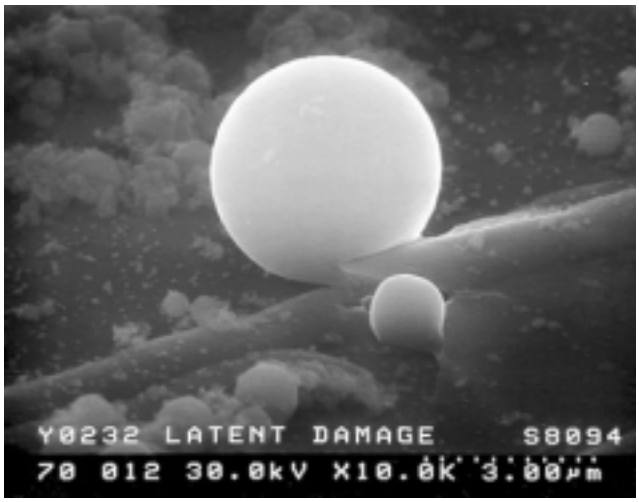

Fig. 2 SEM photo of aluminum spheres emerging from fractured and lifted insulator on a latently damaged National ADC10321.

Metal damage in a contact region was observed in the Cypress oscillator, as shown in Fig. 3. The contact is a via between the first- and second-level metallization layers. The ejected sphere is actually from the top metallization layer. In spite of the size of the sphere, this was actually latent damage. SEM evaluation with EDS showed that the refractory metal that is used to clad the interconnect was still intact. The Cypress oscillator is the only one of the six devices to exhibit damage at contact regions.

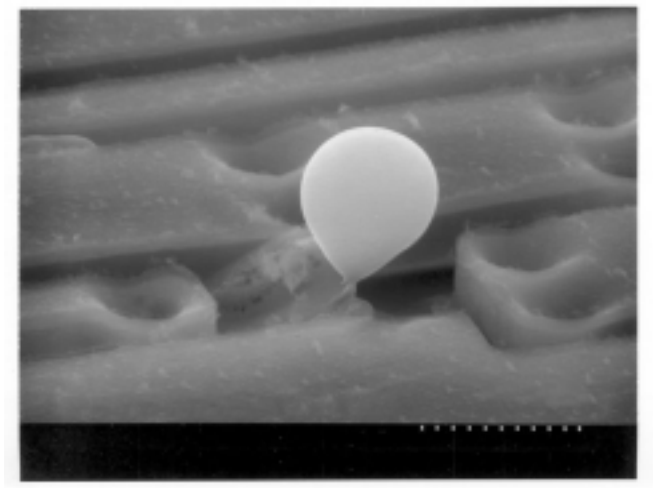

Fig. 3. Scanning electron micrograph of ejected metal at a contact region of the Cypress crystal oscillator.

B. Reproducibility of Damage

Damage results were reproducible with all six tested device types. This was particularly noticeable during laser testing of the AD9260, where we were able to observe damaging events as they occurred and quickly mount fresh devices. Two areas in the analog section of the device were shown to be particularly susceptible to repeatable SEL-induced structural damage. Once these sensitive regions were identified on an initial part, ten additional devices were subjected to laser pulses in the same locations. We observed virtually identical damage signatures in all eleven devices. The damage was approximately 50 percent catastrophic and 50 percent latent. The only differences in the experimental conditions that may have influenced whether or not damage was catastrophic or latent were possible slight variations in the positioning of the laser pulse on different devices.

Similar behavior was observed with the National ADC10321 and the Cypress oscillator. These devices were both tested with Californium-252 fission fragments. SEL-induced damage was reproducible, appeared in the same locations, and was a mixture of catastrophic and latent among individual parts.

C. Key Parameters of Latent Damage

Interconnects are designed to avoid failure from electromigration, which can occur over extended operation if the current density is too high. There is an exponential relationship between current density, failure rate and temperature, but most integrated circuits are designed with maximum current density below 5×10^5 A/cm^2 in order to avoid reliability problems from metallization [8]. If higher current densities occur, then failure occurs in much shorter time periods. For example, electromigration studies on test structures operated at a current density of 1.5×10^7 A/cm^2 showed a mean time to failure of about 100 seconds [9]. Those studies were done on samples that were deposited over a 60 nm SiO_2 layer in order to decrease the thermal resistance of the metallization. Note that insulator thicknesses of about 1000 nm are typically used in integrated circuits. As discussed in the next section, the much higher thermal resistance of a thick insulating region beneath the metallization has a marked effect on the metallization failure properties, and is one reason that current densities for catastrophic failure may differ between different circuit types.

A minimum current density of 10^7A/cm^2 was necessary to produce both catastrophic and latent damage in the studied devices. The range of current densities observed for the three device types that exhibited latent damage was approximately 10^7 to 10^8A/cm^2. These numbers are based on the latchup equilibrium current drawn by the DUT and the cross-sectional area of the damaged interconnect prior to failure (determined during post-test SEM evaluation). Although we do not know the current density in the metallization during normal operation, it is unlikely to exceed the 5×10^5 A/cm^2 limit normally used for VLSI design, and is unlikely to be more than 5% of the current density that occurs during latchup. The pre-damage cross-sectional areas of these interconnects ranged from 1 to 10 square micrometers. Damaging latchup

event durations ranged from 60µs to 18ms. A graph illustrating the current densities and event durations associated with particular device types is presented in Fig.4.

IV. Analysis

A. SEL-Induced Damage Mechanism

Interconnect failures from high current pulses have been studied using simple test structures with feature sizes and insulator thicknesses similar to those of the CMOS devices studied in this paper [10]-[16]. A study by Banerjee et al. [10] of a 4-level metal system subjected to 200ns high current pulses reported open circuit failure and melting of the interconnects in the test structures at current densities of approximately 5 x 10^7A/cm^2 for metal 4 and 6 x 10^7A/cm^2 for metal 1 through 3. Melting was due to resistance increases and corresponding temperature increases within the interconnects of over 1000°C. The events occurred over a long enough duration to be considered steady state and subject to a certain degree of heat dissipation. The study also found that the maximum allowable current density decreased with increasing pulse width.

Our SEM evaluation of damage sites, the magnitudes of damaging current densities, and damaging event durations suggest that a similar mechanism is causing SEL-induced structural damage. High current densities during SEL cause temperature increases in interconnects which lead to melting of metallization and stresses caused by the mismatched thermal expansion coefficients of the metal and insulator material that comprise the interconnect [11]. This stress causes cracking of the insulator which allows melted metal to erupt from the line, often to the point of catastrophic voiding. As the extruded metal cools, it forms into a sphere, the most spatially efficient shape.

B. Rationale for Latent Damage

Interestingly, our data on the current densities and event durations involved for non-destructive latchup events correspond to conditions for failure indicated by previous studies using electrical pulses [10], [12]-[13]. Fig. 4 shows latent damage data for the AD9260, National's ADC10321, and the Cypress oscillator. The time periods for the two converters are the shortest time period for which power could be shut down due to on-board capacitors. For the oscillator, the time period was selected to evaluate catastrophic damage, not latent damage. Latent damage in that device was observed after a series of tests to determine whether catastrophic damage had occurred after about 20 ms, which was dictated by specific requirements of the program that funded the tests.

For comparison, we show the data for interconnect failures from [10] and [12], where the threshold current density for catastrophic failure is 10^7A/cm^2. What is striking is that our current densities are higher and our pulse widths longer than those predicted for failure, and yet we are seeing only latent damage in many devices.

Note that the current density for failure of metallization with 10 µm width was 70% higher for the samples that were deposited on 0.7 micrometer SiO_2 films compared to samples with the same width on 1 micrometer films. This illustrates the importance of thermal resistance on maximum current density. The thermal resistance of interconnects in integrated circuits with several layers of metallization is more complex, and is likely to vary over a considerable range for different device types.

Note also that the reliability studies were done on special test structures with single levels of metallization where the current density and pulse width could be controlled over a broad range. Currents during latchup are essentially set by the I-V characteristics of the particular latchup site, along with series resistance from the power and ground connections. Thus, the current density cannot be adjusted or controlled, only the time period. This restricts the amount of information that can be determined from latchup evaluations of complex circuits compared to test structures. Note also that there is no immediate evidence of latent damage when these tests are done. Latent damage can only be determined by detailed examination of the device surface with a scanning electron microscope after latchup testing is completed.

Another important point is that the latchup results in Fig. 4 are for three different circuits with multiple metallization levels. The ADC10321 had three metal levels, while the AD9260 and Cypress oscillator had two. The thickness of the oxide (or nitride) layers between the metallization regions was different as well. The thermal resistance of these devices is clearly different, so one should not draw conclusions about current density/pulse width dependences by comparing results for the different circuits. Fig. 4 is intended to illustrate that the current densities where we observe latent damage are within the same range that is observed for detailed studies of failures in isolated metallization test structures.

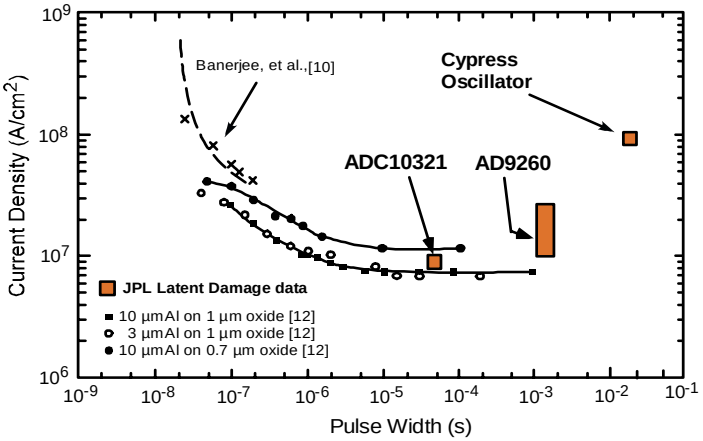

Fig. 4. Latent damage data compared with conditions for interconnect failure from studies in [10] and [12].

Our SEM analysis suggests several reasons why some damaging latchup events are not catastrophic. The amount of released metal may simply be too small to cause complete interconnect voiding and device failure. Another possibility is that barrier metal between the aluminum and insulator material may remain intact after voiding of the aluminum in some interconnects. This cladding may maintain electrical continuity [17] following a damaging SEL event. The latently damaged device in Fig. 1 could have remained functional for this reason (note the thin "rails" that bridge the voided region).

More dramatically, after melting and re-crystallization, some metal may form a bridge across the void, keeping the circuit closed and causing only non-catastrophic damage. This is illustrated in Fig. 5. However, the interconnect cross-section in the damaged region may be significantly smaller than originally intended for normal operating conditions and more susceptible to later failures, either from subsequent latchup events or electromigration.

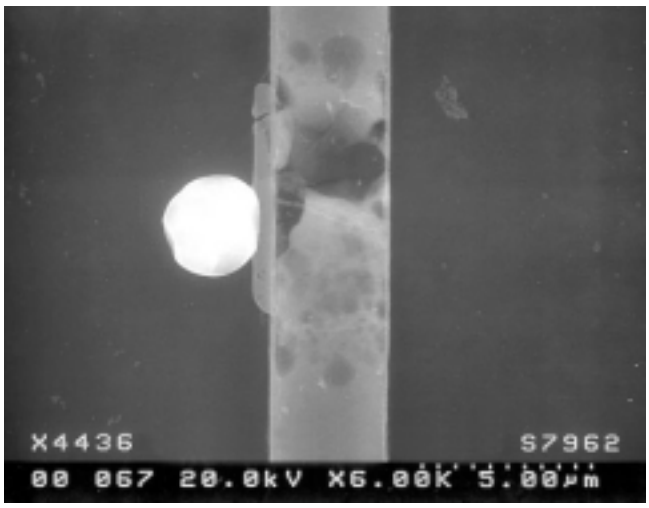

Fig. 5. A latently damaged AD9260 interconnect with an aluminum "bridge" across a void.

V. Discussion

A. Reliability Issues

Although the best approach in dealing with latchup is to avoid using devices that are sensitive to latchup from heavy ions or protons, this is not always possible, and some space systems permit the use of latchup-sensitive parts with special mitigation circuitry. The latent damage effects from SEL presented in this paper introduce a reliability hazard that has not been previously considered from the standpoint of latchup mitigation. Fig. 1 and Fig. 5 show that SEL can cause interconnect cross-sections to be reduced by approximately 1 to 2 orders of magnitude (in the small region where metallization is ejected) without affecting DUT functionality. The resistance increase caused by these smaller cross-sections can potentially increase the chances of failure from subsequent latchup events where current densities would be expected to be even higher than before latent damage occurred.

Vulnerability to electromigration damage is another concern. Localized melting and re-crystallization of metal lines can result in a reduction of grain size and the creation of a larger number of grain boundaries in the interconnects [14]. This can lead to electromigration-related damage, and may contribute to long-term reliability problems for parts that have sustained SEL-induced latent damage.

An additional danger is introduced for devices that do not have encapsulating plastic packaging, such as the ceramic packaging of the ADSP2100 where an air gap exists between the chip and a metal lid. Extruded metal or dislodged metal spheres from latent damage could potentially cause a short circuit by coming in contact with other wiring.

It is also important to note that, although the focus of this study is on CMOS devices, other technologies may exhibit similar metallization damage signatures if very high current density situations occur during their operation.

B. Effect on Future SEL Mitigation Efforts

This paper shows that SEL-induced latent damage is not an isolated incident associated with only one CMOS device type. Three of the 6 device types studied have shown latent damage, indicating that it may be a pervasive problem.

Our first observation of SEL-induced structural damage was during laser testing, which allowed direct, microscopic observation of the delidded DUT. Such monitoring would not have been possible at an accelerator facility. Since latent damage causes no obvious change in device functionality, we would not have known that latently damaging SEL's had occurred at an accelerator unless subsequent surface analysis were done. Efforts to design hardware or software for latchup mitigation should include considerations for possible latent damage events which may be hard to observe and may take place over very short time periods. As the study by Banerjee et al. illustrated, such damage can occur in under 200ns. The range of damaging event durations presented in our study represents typical timing involved with existing detection and crowbar circuitry. However, as our study has shown, the absence of electrical "symptoms" does not necessarily imply that a device has not been damaged during a mitigated SEL.

Typically, the goal of SEL testing for mitigation circuit design is to avoid failure so that the latchup cross section can be measured. A test circuit that includes some SEL detection and power shutdown is usually used, and a histogram of the distribution of SEL current levels is generated. This method may overlook quickly occurring latent damage events that may not be mitigated by the final design. Although we were unable to shut down power at time periods less than about 60

µs for any of the circuits that we studied, pulsed metallization studies in the literature suggest that one would have to shut down latchup in time periods of 1 µs or less in order to avoid latent damage. This is a much shorter time period than is usually considered for latchup mitigation circuitry.

Latchup mitigation is a complex problem because there are often large numbers of internal latchup sites with different currents during latchup. Latchup testing with current shutdown must include enough different latchup events to verify that the mitigation is effective for a large number of latchup paths on a given device, which is difficult and time consuming. Fig. 6 shows an example of catastrophic metallization damage in the DSP-2100. A series of tests on this device showed that catastrophic damage could be eliminated by removing power within 1 ms, but that damage was catastrophic for about 30% of the events when latchup was shutdown after 300 ms (those time intervals were dictated by a specific space system that used latchup circumvention for this device). This device had a large number of internal latchup sites, with equilibrium latchup currents that ranged from 50 mA to > 2A. Catastrophic damage was only observed for events with currents above 300 mA, consistent with the threshold current density range of the other devices in the study. The complexity of the DSP-2100 and the presence of so many different latchup paths made it difficult to evaluate latchup in this device.

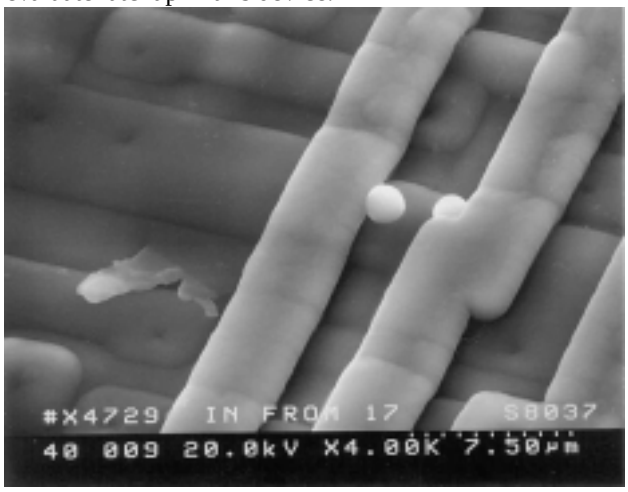

Fig. 6. Metallization damage in the DSP-2100 after catastrophic failure. The latchup current was 2 A.

C. Next-Generation Devices

The evolution of devices and processing technologies since the early 1980's has resulted in smaller feature sizes and increased numbers of levels of metal [17]. For a given current density, modeling has shown that, for multi-level systems, the top level of metal experiences the highest temperature increase, and this temperature increases as more levels of metal are used [15]. One possible reason for this is relative distance from the silicon substrate heat sink [16].

Reference [15] also addresses Joule heating issues in newer copper metallization and low-dielectric constant (k) inter-level dielectrics. Although copper has a lower resistivity than aluminum and exhibits less Joule heating for a given current density, copper interconnects may be expected to be smaller and to carry higher current densities than aluminum has in the past. Additionally, compared to SiO_2, low-k dielectrics have low thermal conductivities, and may adversely affect heat dissipation during high current density events.

The trend toward smaller feature sizes and even more densely packed levels of interconnects is expected to continue. Therefore, it is possible that next generation devices may have a higher incidence of the type of SEL-induced catastrophic and latent damage presented in this paper. Unfortunately, as the number of metal layers increases it will become increasingly difficult to diagnose latent damage in the lower levels of metal, because it may be obstructed by the top metal layers. Conventional practice for VLSI circuit design is to use conductors with large cross section in top layers, decreasing the cross sectional area for the metal layers below the surface. Thus, latent (or catastrophic) damage may be more likely in lower layers that are designed to carry much lower currents during normal operation compared to the high currents that occur during latchup.

VI. Conclusions

This paper demonstrates that for a variety of CMOS devices, high current density conditions during single-event latchup may produce non-catastrophic interconnect damage from melting. Because this type of structural damage is permanent and significantly reduces interconnect cross-sections in the damaged area, it raises a concern about vulnerability to future device failure due to electromigration or additional SEL events.

Future latchup circumvention efforts should take this type of damage into account, especially since it often occurs over very short time periods and is difficult to observe without some form of surface analysis. Next generation devices are expected to contain smaller interconnects and more levels of metallization, and therefore may be more prone to damaging temperature increases and to the type of latent and catastrophic damage presented in this study.

Small ejected metal spheres emerged as a signature for identifying this type of damage. Reliability data in the literature and our test results show that the threshold current density for damage is 10^7 A/cm^2.

VII. Acknowledgments

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